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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/520,121	08/31/2005	Christian Bussiere	37114-212314	2539

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EXAMINER	
LEVI, DAMEON E	

ART UNIT	PAPER NUMBER
2841	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/520,121	BUSSIERE ET AL.	
	Examiner	Art Unit	
	DAMEON E. LEVI	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/03/2005(NEW APP)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-32* is/are rejected.

7)☒ Claim(s) *11 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/03/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-10, and 12-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Azoulay et al US Patent 7030830.

Regarding claim 1, Azoulay et al discloses a structure comprising:

a wall assembly(element 16, 18,Figs 1-27) mounted on said electronic IC(column 9, lines 33-45) and

having at least one wall surface(element 20,22,Figs 1-27) extending from the IC so as to be aligned with a target area on the electrical pad; said target area being sufficiently large to receive an antenna terminal(element 14, Figs 1-27) of a radio-frequency

identification device; whereby abutting said antenna terminal against said at least one wall surface allows positioning the antenna terminal on the electrical pad.

Regarding claim 2, Azoulay et al discloses wherein the electrical pad is composed of first and second miniature pads(elements 24,26, Figs 1-27) internally electrically connected together, and so positioned relative to each other as to yield an inter-spacing between them; said target area being positioned within said inter-spacing; said wall assembly including a first wall(1st element 20, Figs 1-27), defining a first wall surface, mounted on said first miniature pad adjacent said target area on a first side thereof so that said first wall surface is aligned with the target area.

Regarding claim 3, Azoulay et al discloses wherein said wall assembly further includes a second wall (2nd element 20, Figs 1-27), defining a second wall surface, mounted adjacent said target area on said second miniature pad opposite said first side of the target area so as to be aligned with said target area.

Regarding claim 4, Azoulay et al discloses wherein said wall assembly further includes a second wall (element 22, Figs 1-27), mounted on a protective layer of said electronic circuit surface on the same side as said first side relatively to the target area; said second wall being so configured and sized as to define a second wall surface aligned with said target area.

Regarding claim 5, Azoulay et al discloses said wall assembly includes a rectangular body (element 28, Figs 1-27), extending from the electronic circuit surface.

Regarding claim 6, Azoulay et al discloses said at least one wall surface includes two opposite surfaces defining a groove generally aligned with said pad (groove between elements 20, Figs 1-27).

Regarding claim 7, Azoulay et al discloses wherein said two opposite surfaces are two facing concave surfaces (groove between elements 20, Figs 1-27).

Regarding claim 8, Azoulay et al discloses wherein said two opposite surfaces are two facing skew surfaces, defining a tapered groove generally aligned with said target area on the electrical pad (tapered elements a6, a5, Figs 1-27).

Regarding claim 9, Azoulay et al discloses wherein each of said two opposite wall surfaces extends generally perpendicularly, from the electronic circuit surface (elements 20, Figs 1-27).

Regarding claim 10, Azoulay et al discloses wherein said wall assembly includes two spaced hemispheres, each defining a surface that is tangentially aligned with said target area (elements 20, Figs 1-27).

Regarding claim 12, Azoulay et al discloses wherein said wall assembly is made from a material deposited on the electronic IC (column 9, lines 33-45).

Regarding claim 13, Azoulay et al discloses wherein said material deposited on the electronic IC is selected from the group consisting of polymide and ultra-violet glue (column 9, lines 33-45).

Regarding claim 14, Azoulay et al discloses wherein said material is electrically conductive (column 9, lines 33-45).

Regarding claim 15, Azoulay et al discloses wherein said material is electrically non-conductive (column 9, lines 33-45).

Regarding claim 16, Azoulay et al discloses wherein said wall assembly includes a first wall, defining a first wall surface(1st element 20, Figs 1-27) mounted on the electrical pad adjacent the target area on a first side thereof so that said first wall surface is aligned with the target area.

Regarding claim 17, Azoulay et al discloses wherein said wall assembly further includes a second wall (2nd element 20, Figs 1-27), defining a second wall surface, mounted adjacent said target area on a second side opposite said first side of the target area so as to be aligned with said target area.

Regarding claim 18, Azoulay et al discloses wherein said wall assembly further includes a second wall (element 22, Figs 1-27) mounted on a protective layer of said electronic circuit surface on the same side as said first side relatively to the electrical pad; said second wall being so configured and sized as to define a second wall surface aligned with said target area.

Regarding claim 19, Azoulay et al discloses wherein said first wall is triangular prism-shaped and said second wall surface is convex and is substantially tangentially aligned with the target area(1st element 20, Figs 1-27).

Regarding claim 20, Azoulay et al discloses wherein said geometry structure is mounted on a protective layer on said electronic circuit surface (column 9, lines 33-45).

Regarding claim 21, Azoulay et al discloses wherein said wall assembly includes two facing concave surfaces extending generally perpendicularly from the electronic IC so as to be generally aligned with said target area (element 16, 18, Figs 1-27).

Regarding claim 22, Azoulay et al discloses wherein said electronic IC is selected from the group consisting of a radio- frequency identification device microchip, a micro sensor microchip or and micro electronic machine (MEM) (column 9, lines 33-45, Abstract).

Regarding claims 23-32, it is the position of the Office that the methods disclosed therein are deemed as being inherent in the assembly of the apparatus as claimed in the preceding claims since the prior art apparatus is deemed as teaching or suggesting the structural elements as recited in the methods.

The claims are thus subsequently rejected.

Allowable Subject Matter

Claims 11 and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art cannot be construed as adequately teaching or suggesting wherein the radio-frequency identification device have two electrical pads; said wall assembly includes two external rectangular-shaped portions and an internal generally square-shaped portion made of an electrically non-conductive material; said two external,

rectangular-shaped portions and said internal generally square-shaped portion being generally parallel and being consecutively distanced so as to yields two interspaces that are generally aligned with a respective target area(as recited in dependent claim 11), or, wherein said wall assembly includes two opposite parallel walls extending from said electronic circuit surface defining a groove generally aligned with said pad;
each of said two opposite parallel walls having a top surface parallel to said surfaces; contacting the antenna terminal with said at least one wall surface is achieved by swiping the antenna terminal onto said top surfaces of said two opposite parallel walls until the antenna terminal engages said groove(as recited in dependent claim 33).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAMEON E. LEVI whose telephone number is (571)272-2105. The examiner can normally be reached on Mon.-Thurs. (9:00 - 5:00) IFP, Fridays Telework.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on (571) 272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dameon E Levi
Examiner
Art Unit 2841

/Dameon E Levi/
Examiner, Art Unit 2841